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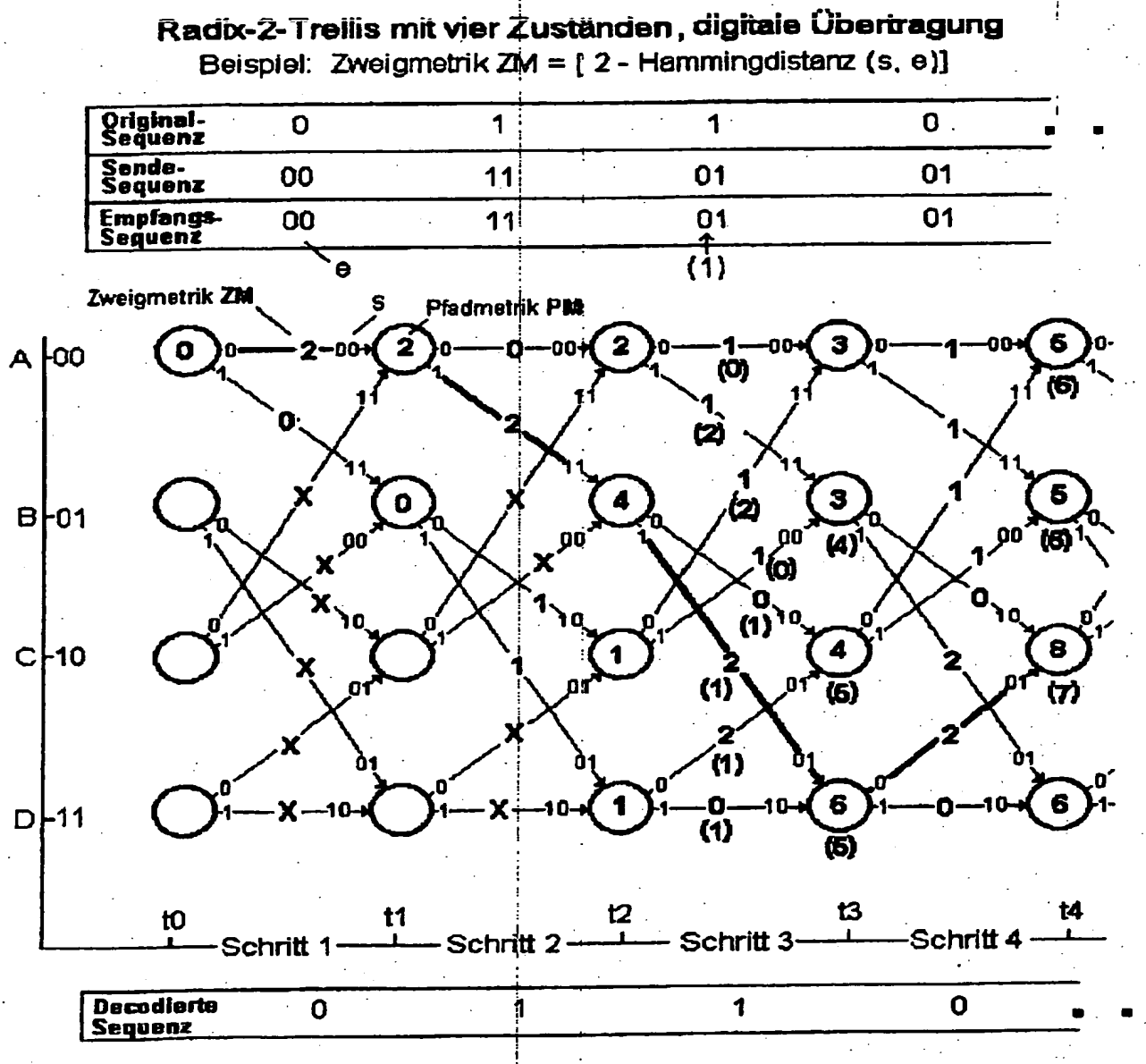
Radix-2-Trellis mit vier Zuständen, digitale Übertragung
Beispiel: Zweigmetrik ZM = [2 - Hammingdistanz (s, e)]
Original-Sequenz 0 1 1 0
Sende-Sequenz 00 11 01 01
Empfangs-Sequenz 00 11 01 01
e
(1)
Zweigmetrik ZM
s
Pfadmetrik PM
A 00
B 01
C 10
D 11
t0 t1 t2 t3 t4
Schritt 1 Schritt 2 Schritt 3 Schritt 4
Decodierte Sequenz 0 1 1 0

FIG. 1

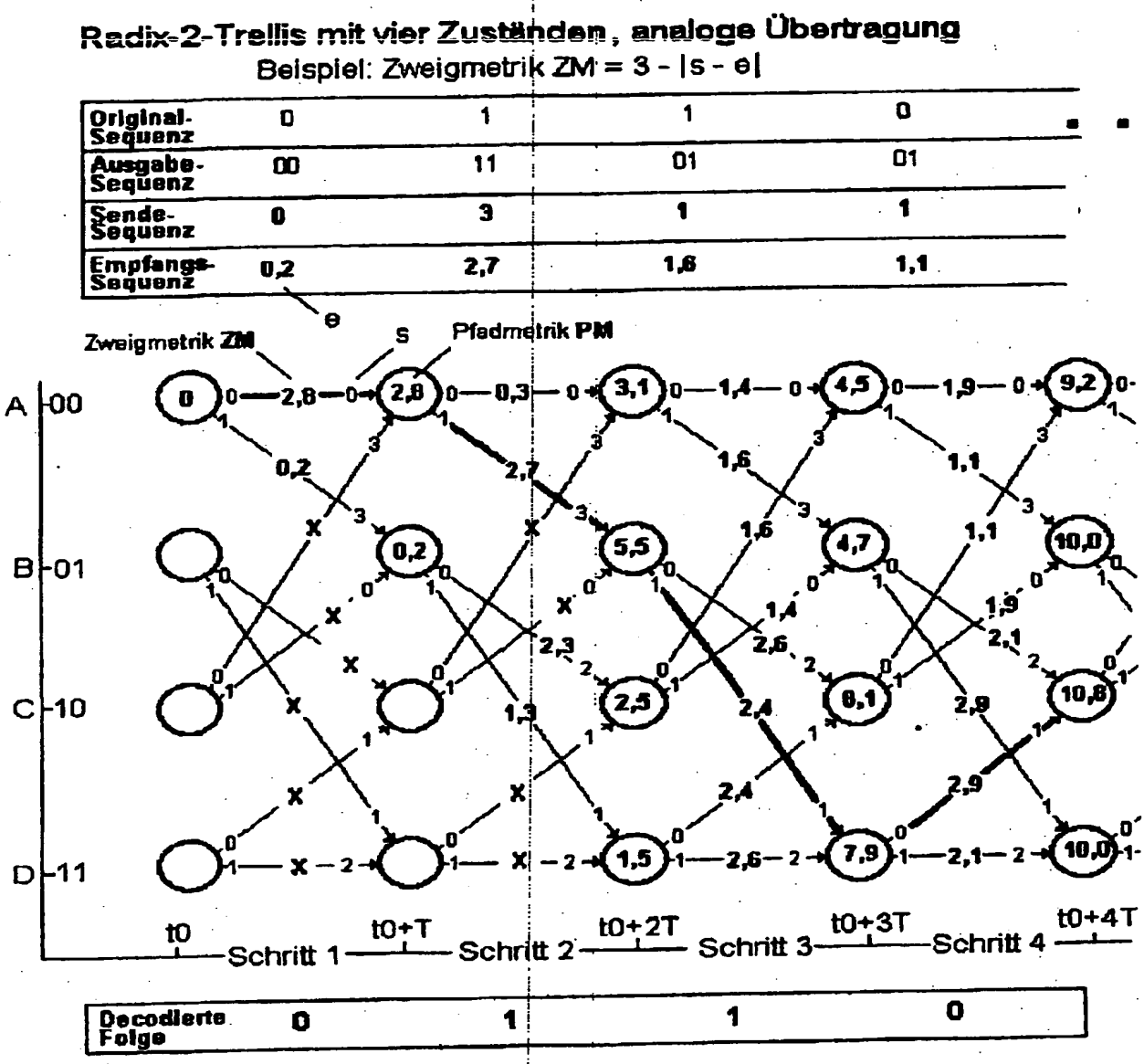
Radix-2-Trellis mit vier Zuständen, analoge Übertragung
Beispiel: Zweigmetrik ZM = 3 - |s - e|
Original-Sequenz 0 1 1 0
Ausgabe-Sequenz 00 11 01 01
Sende-Sequenz 0 3 1 1
Empfangs-Sequenz 0,2 2,7 1,6 1,1
e
s
Zweigmetrik ZM
Pfadmetrik PM
A 00
B 01
C 10
D 11
t0
t0+T
t0+2T
t0+3T
t0+4T
Schritt 1
Schritt 2
Schritt 3
Schritt 4
Decodierte Folge 0 1 1 0

FIG. 2

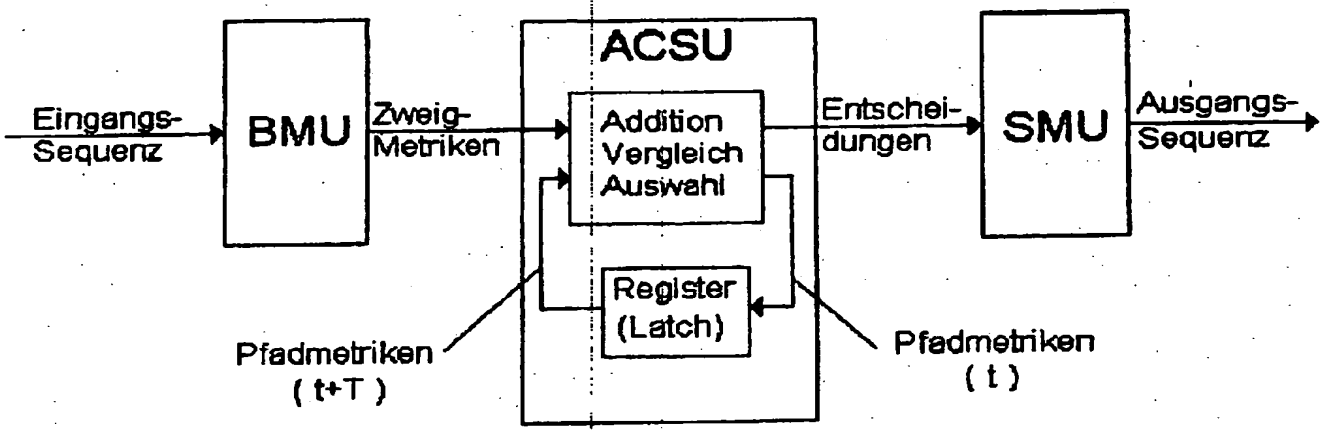
ACSU
Eingangs-
Sequenz
BMU
Zweig-
Metriken
Addition
Vergleich
Auswahl
Register
(Latch)
Pfadmetriken
(t+T)
Pfadmetriken
(t)
Entschei-
dungen
SMU
Ausgangs-
Sequenz

FIG. 3

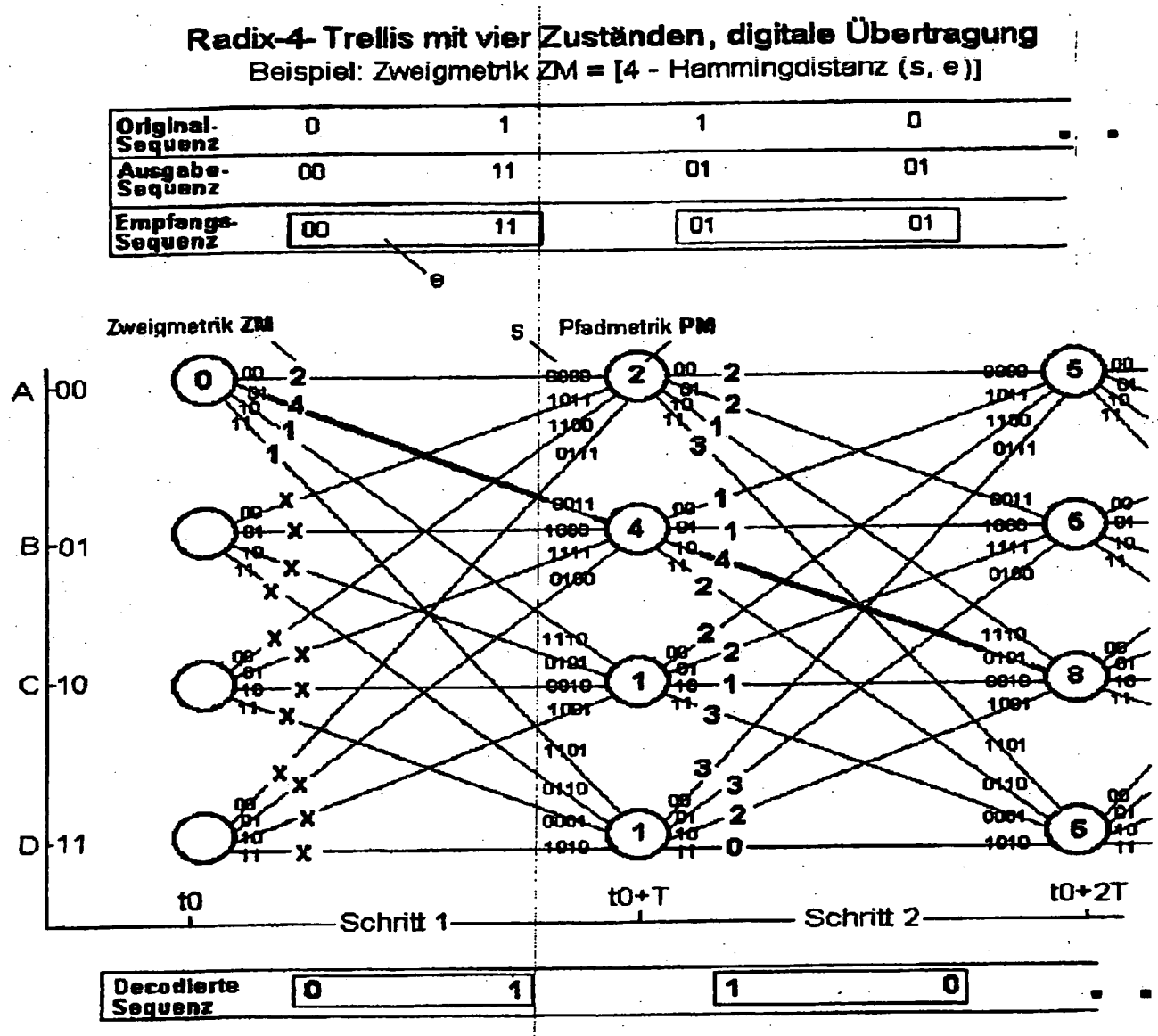
Radix-4- Trellis mit vier Zuständen, digitale Übertragung
Beispiel: Zweigmetrik ZM = [4 - Hammingdistanz (s, e)]
Original-Sequenz 0 1 1 0
Ausgabe-Sequenz 00 11 01 01
Empfangs-Sequenz 00 11 01 01
e
Zweigmetrik ZM
s
Pfadmetrik PM
A 00
B 01
C 10
D 11
t0
t0+T
t0+2T
Schritt 1
Schritt 2
Decodierte Sequenz 0 1 1 0

FIG. 4

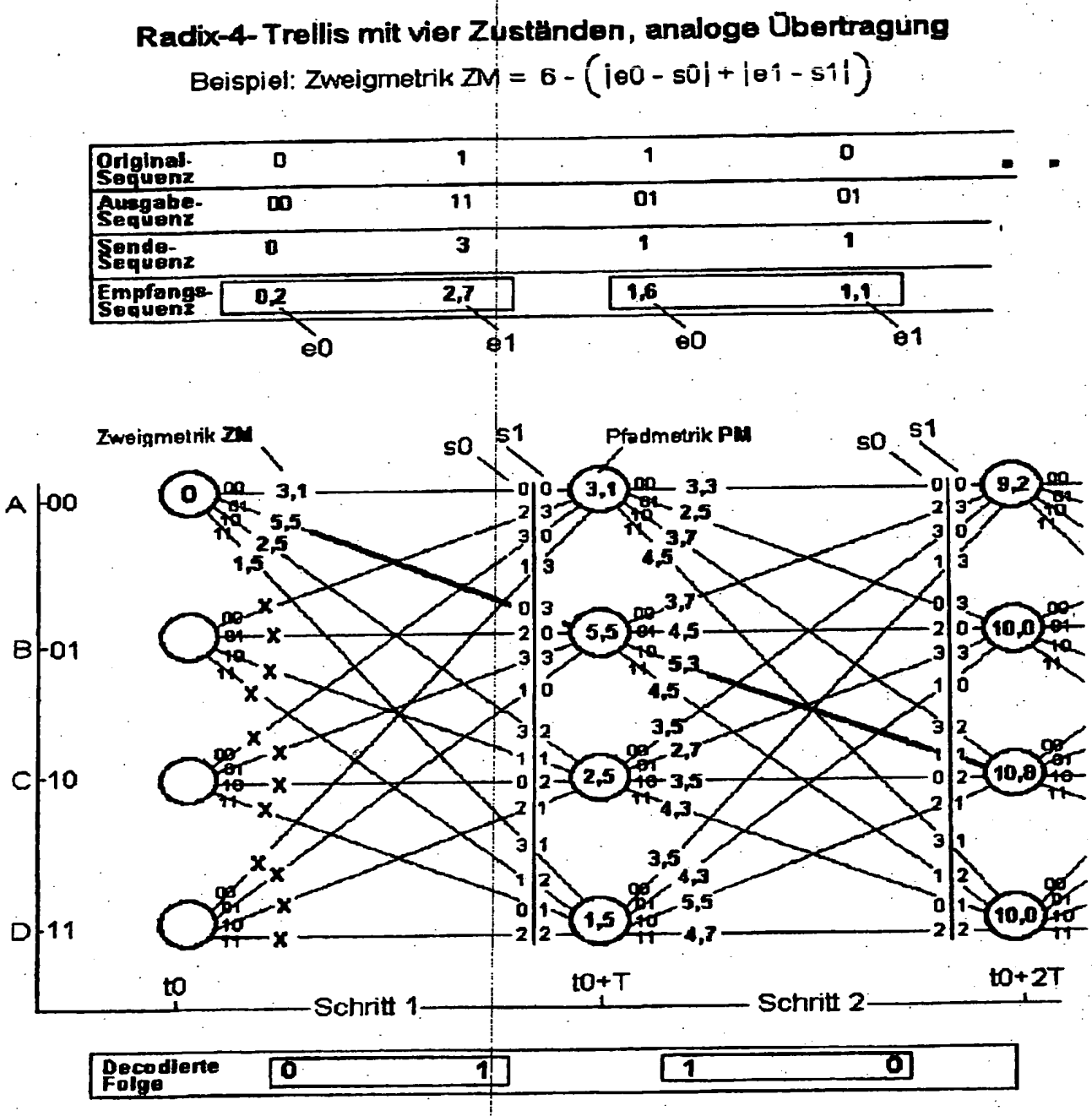
Radix-4-Trellis mit vier Zuständen, analoge Übertragung
Beispiel: Zweigmetrik ZM = 6 - (|e0 - s0| + |e1 - s1|)
Original-Sequenz 0 1 1 0
Ausgabe-Sequenz 00 11 01 01
Sende-Sequenz 0 3 1 1
Empfangs-Sequenz 0,2 2,7 1,6 1,1
e0 e1 e0 e1
Zweigmetrik ZM
Pfadmetrik PM
s0 s1
A 00
B 01
C 10
D 11
t0 t0+T t0+2T
Schritt 1 Schritt 2
Decodierte Folge 0 1 1 0

FIG. 5

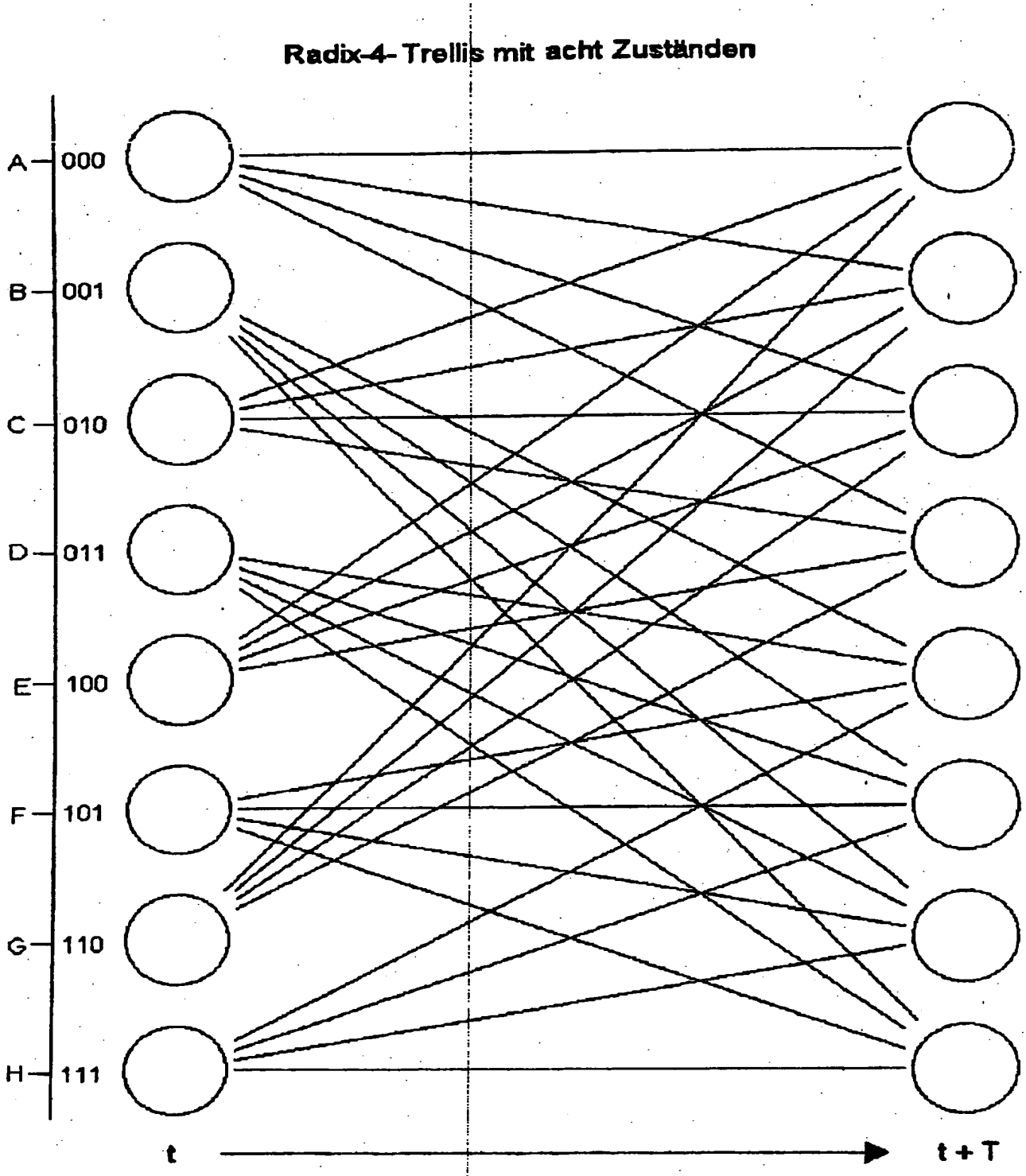
Radix-4- Trellis mit acht Zuständen
A
000
B
001
C
010
D
011
E
100
F
101
G
110
H
111
t
t + T

FIG. 6

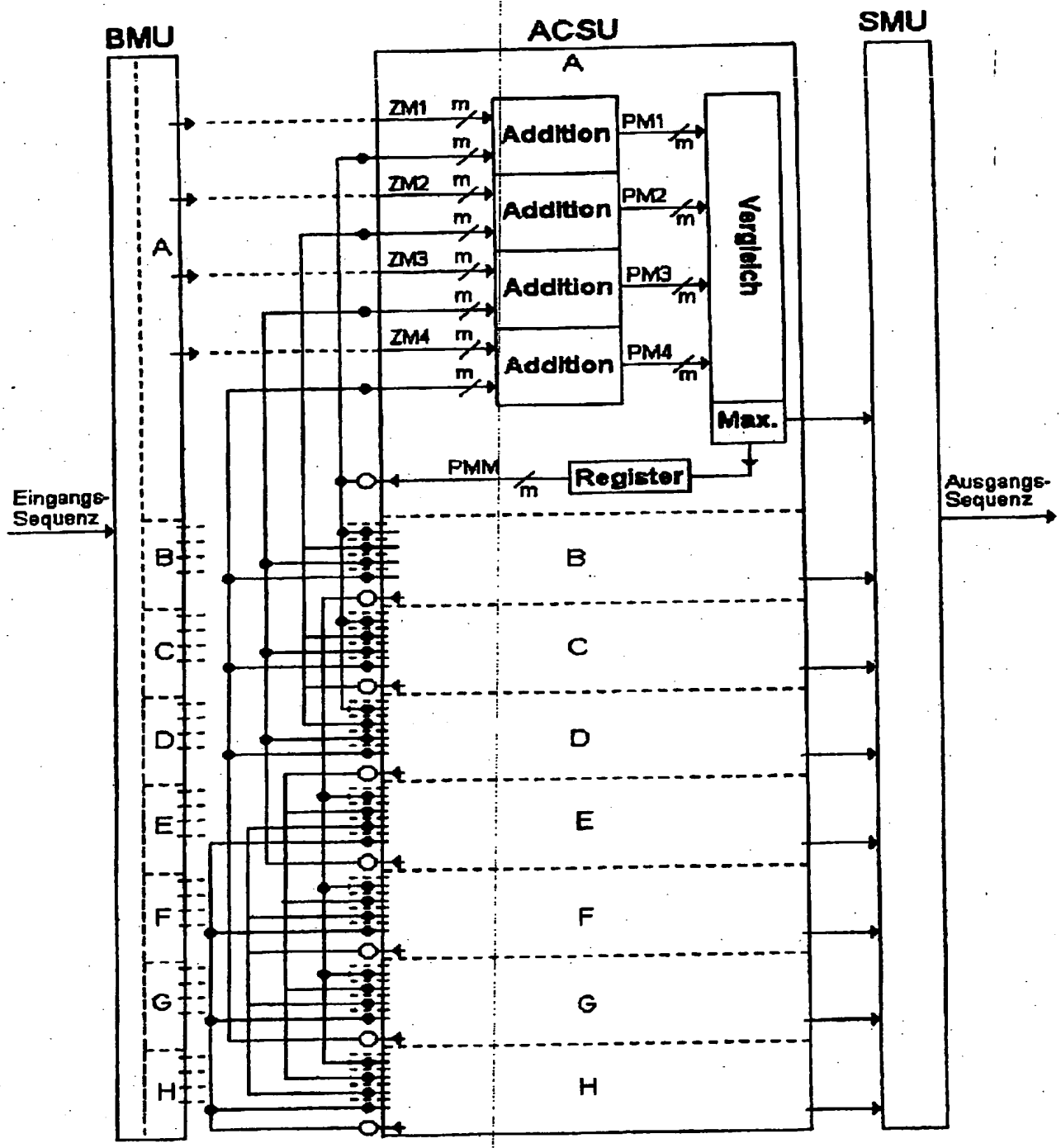
BMU
ACSU
A
SMU
ZM1
ZM2
ZM3
ZM4
m
Addition
Addition
Addition
Addition
PM1
PM2
PM3
PM4
Vergleich
Max.
PMM
Register
Eingangs-Sequenz
Ausgangs-Sequenz
A
B
C
D
E
F
G
H

FIG. 7

ACSU-Abteilung A aus Fig. 7

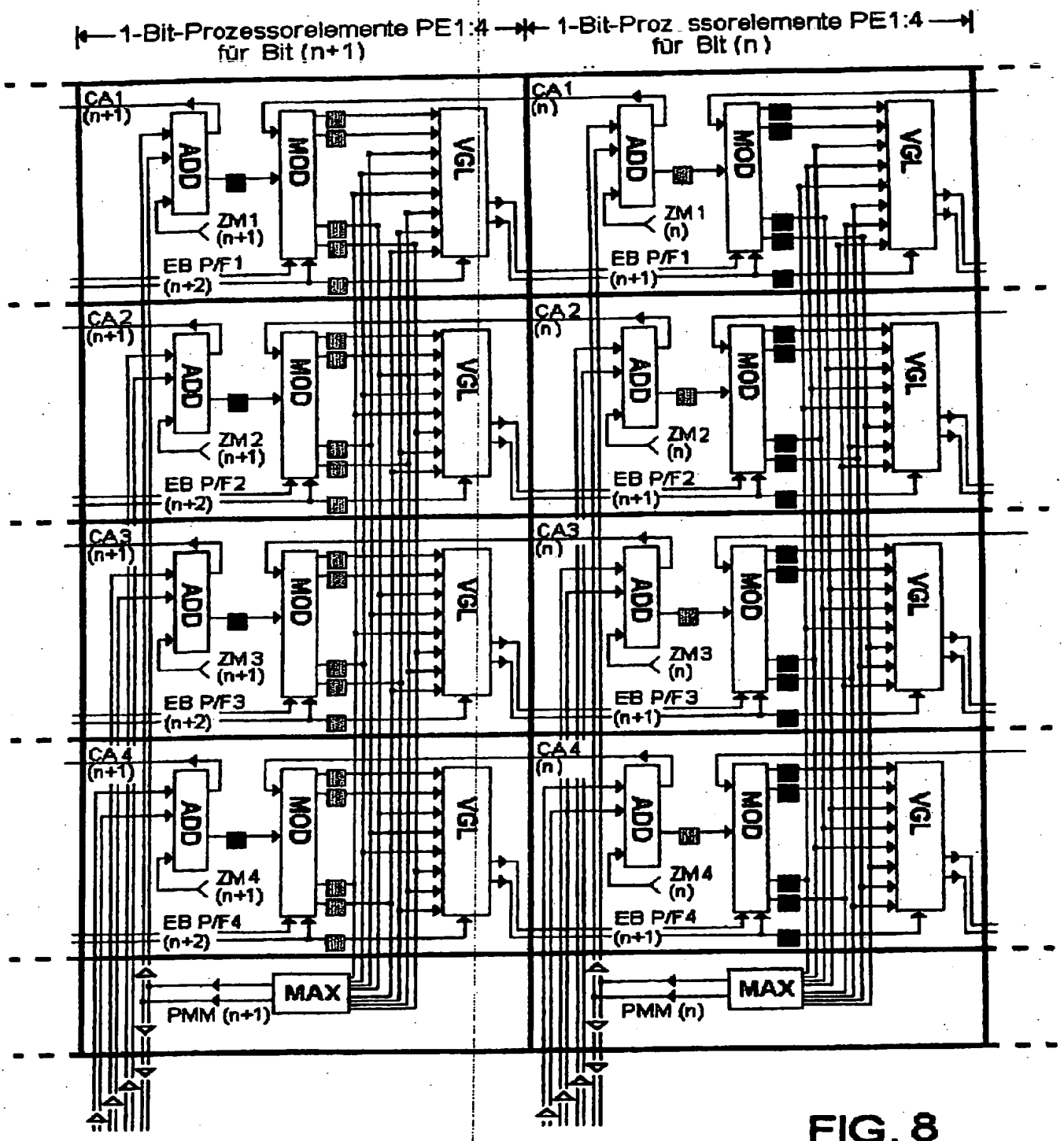

FIG. 8
Stand der Technik

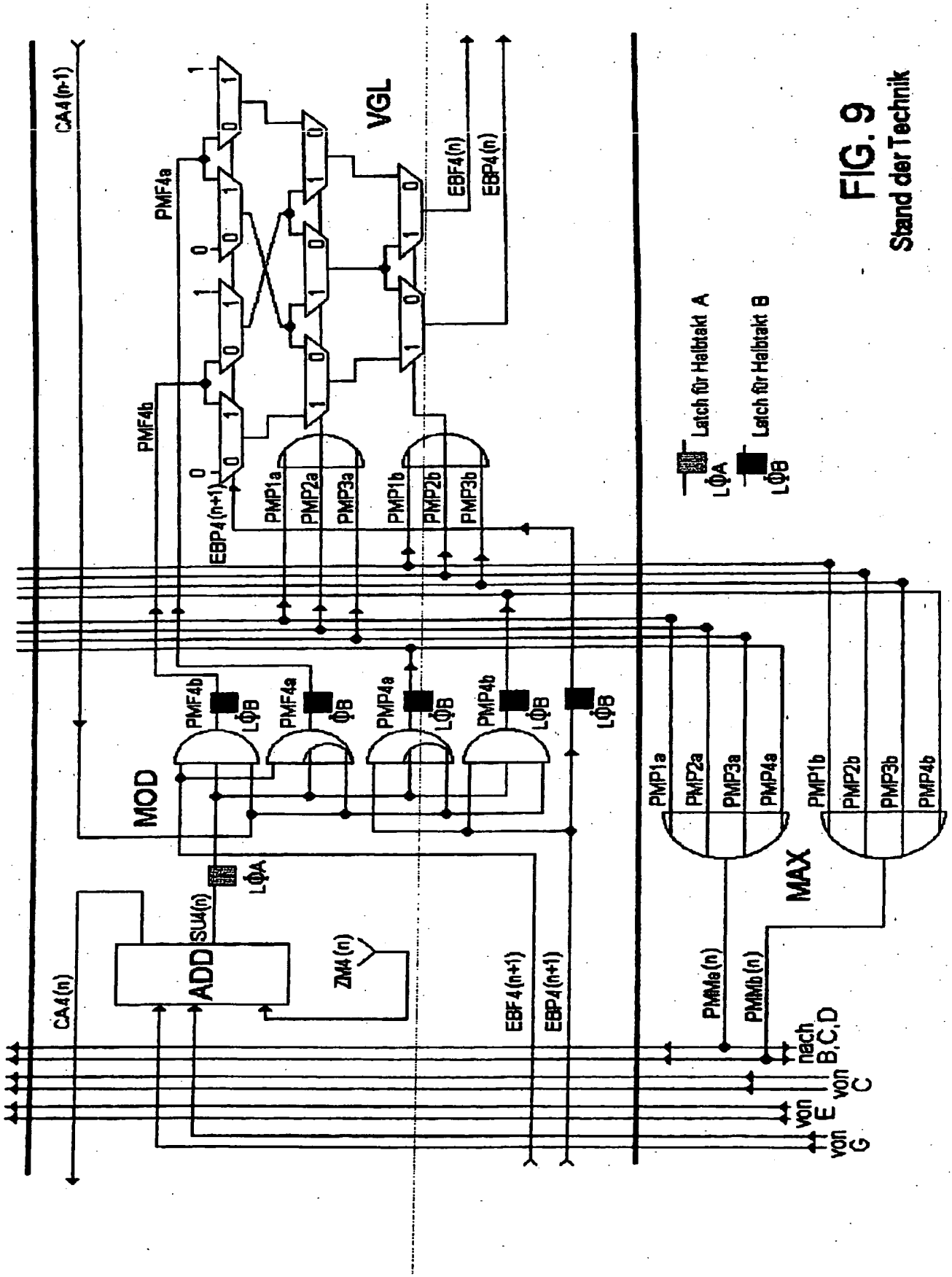

FIG. 9
Stand der Technik

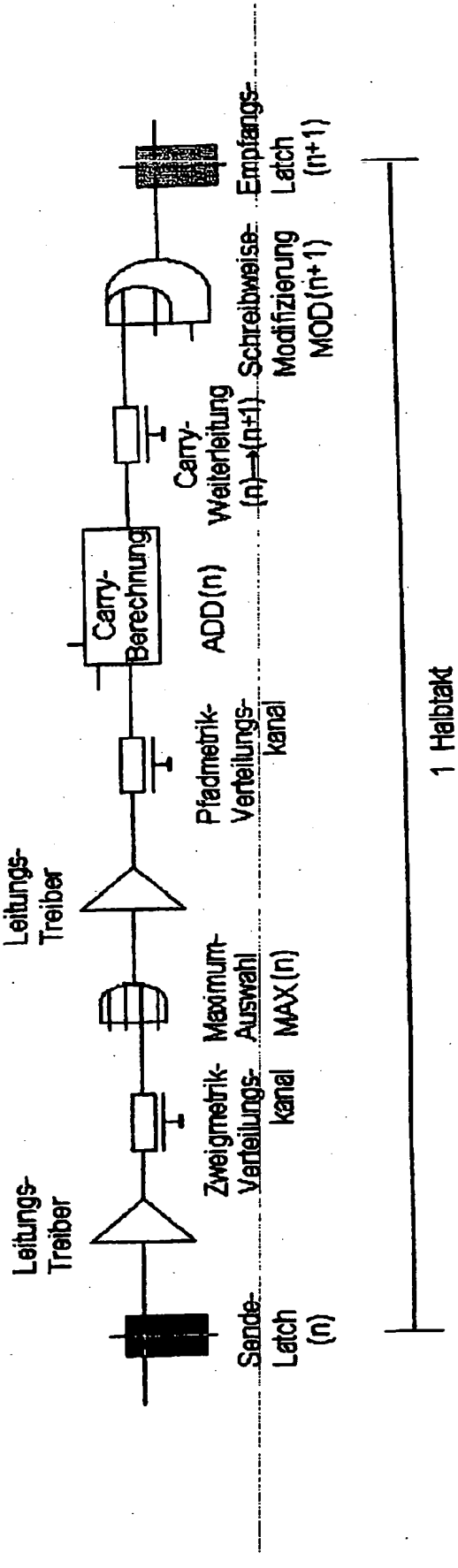

FIG.10
Stand der Technik

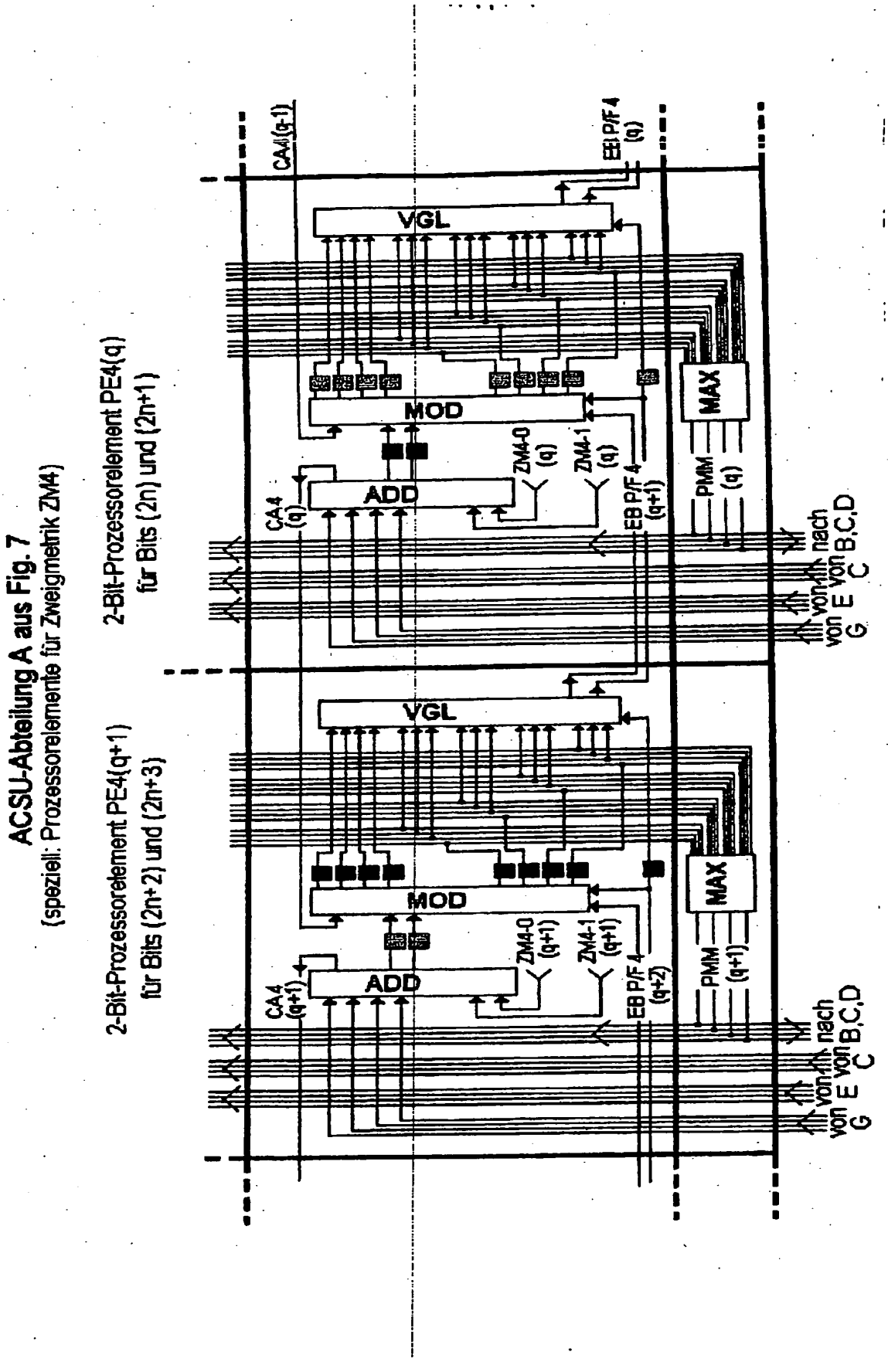
ACSU-Abteilung A aus Fig. 7
(speziell: Prozessorelemente für Zweigmetrik ZM4)
2-Bit-Prozessorelement PE4(q+1)
für Bits (2n+2) und (2n+3)
2-Bit-Prozessorelement PE4(q)
für Bits (2n) und (2n+1)
CA4(q-1)
EB P/F 4 (q)
VGL
MOD
ADD
MAX
ZM4-0 (q)
ZM4-1 (q)
CA4 (q)
EB P/F 4 (q+1)
PMM (q)
von E nach G von C B,C,D
ZM4-0 (q+1)
ZM4-1 (q+1)
CA4 (q+1)
EB P/F 4 (q+2)
PMM (q+1)

FIG. 11

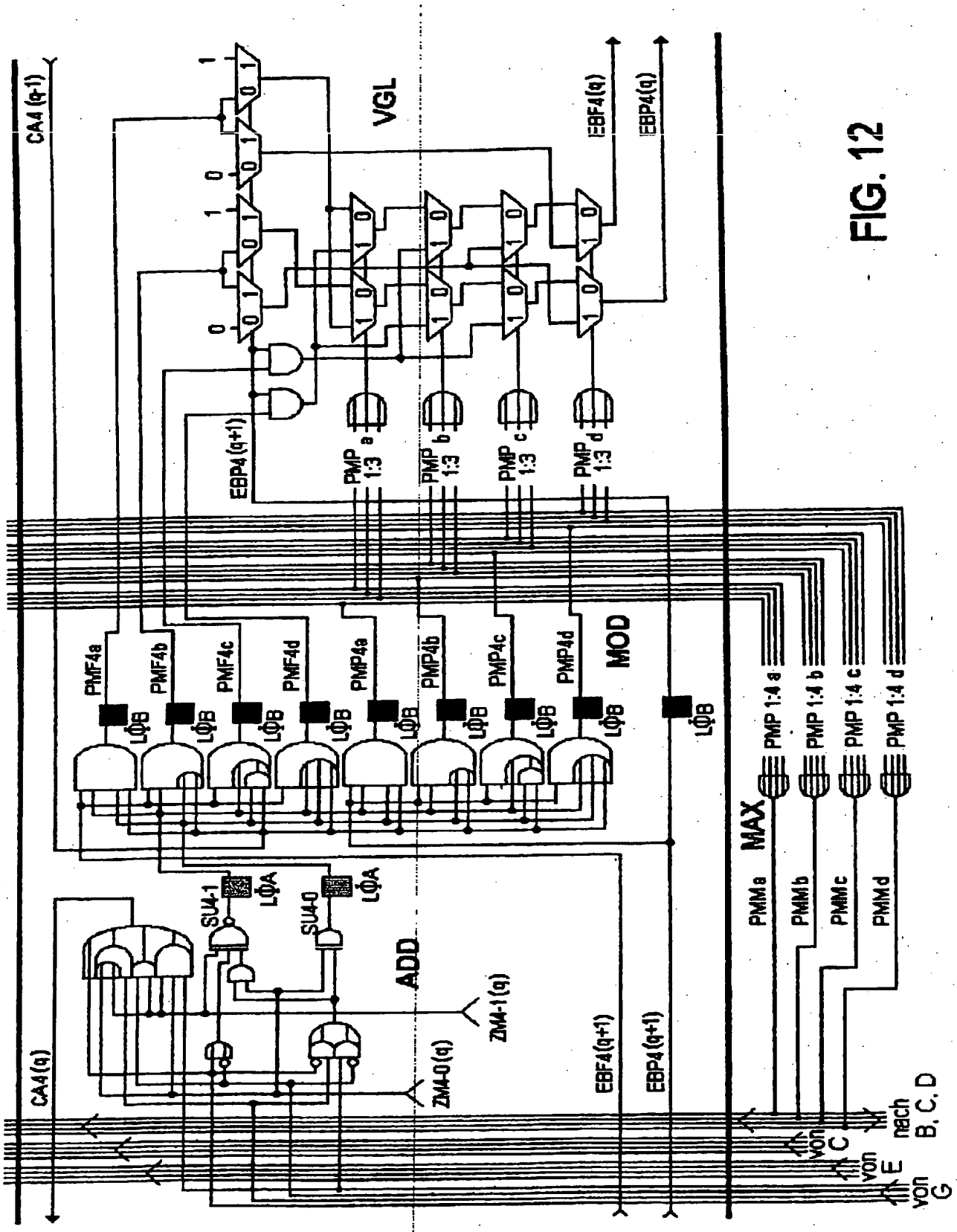
CA4 (q-1)
VGL
EBF4(q)
EBP4(q)
EBP4 (q+1)
PMP 1:3 a
PMP 1:3 b
PMP 1:3 c
PMP 1:3 d
PMF4a
PMF4b
PMF4c
PMF4d
PMP4a
PMP4b
PMP4c
PMP4d
MOD
LΦB
PMP 1:4 a
PMP 1:4 b
PMP 1:4 c
PMP 1:4 d
MAX
PMMa
PMMb
PMMc
PMMd
SU4-1
SU4-0
LΦA
ADD
ZM4-1(q)
ZM4-0(q)
EBF4(q+1)
EBP4(q+1)
CA4(q)
von C nach B, C, D
von E
von G

FIG. 12

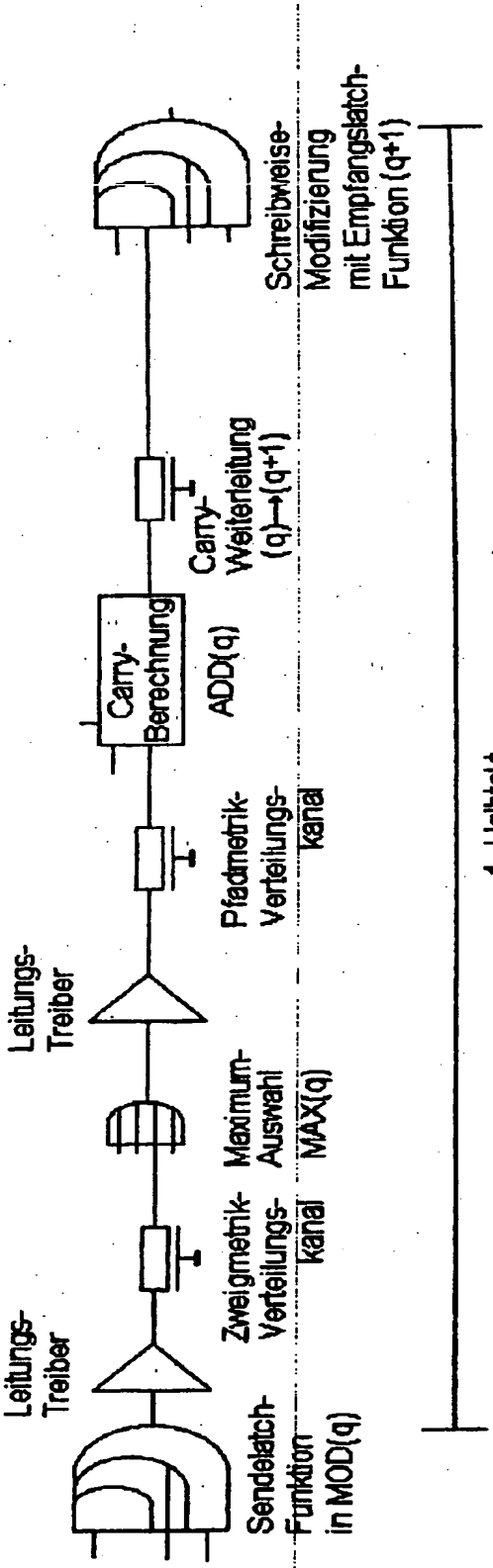
Schreibweise-
Modifizierung
mit Empfangslatch-
Funktion (q+1)
Carry-
Weiterleitung
(q)→(q+1)
Carry-
Berechnung
ADD(q)
Pfadmetrik-
Verteilungs-
kanal
Leitungs-
Treiber
Maximum-
Auswahl
MAX(q)
Zweigmetrik-
Verteilungs-
kanal
Leitungs-
Treiber
Sendelatch-
Funktion
in MOD(q)
1 Halbtakt

FIG. 13

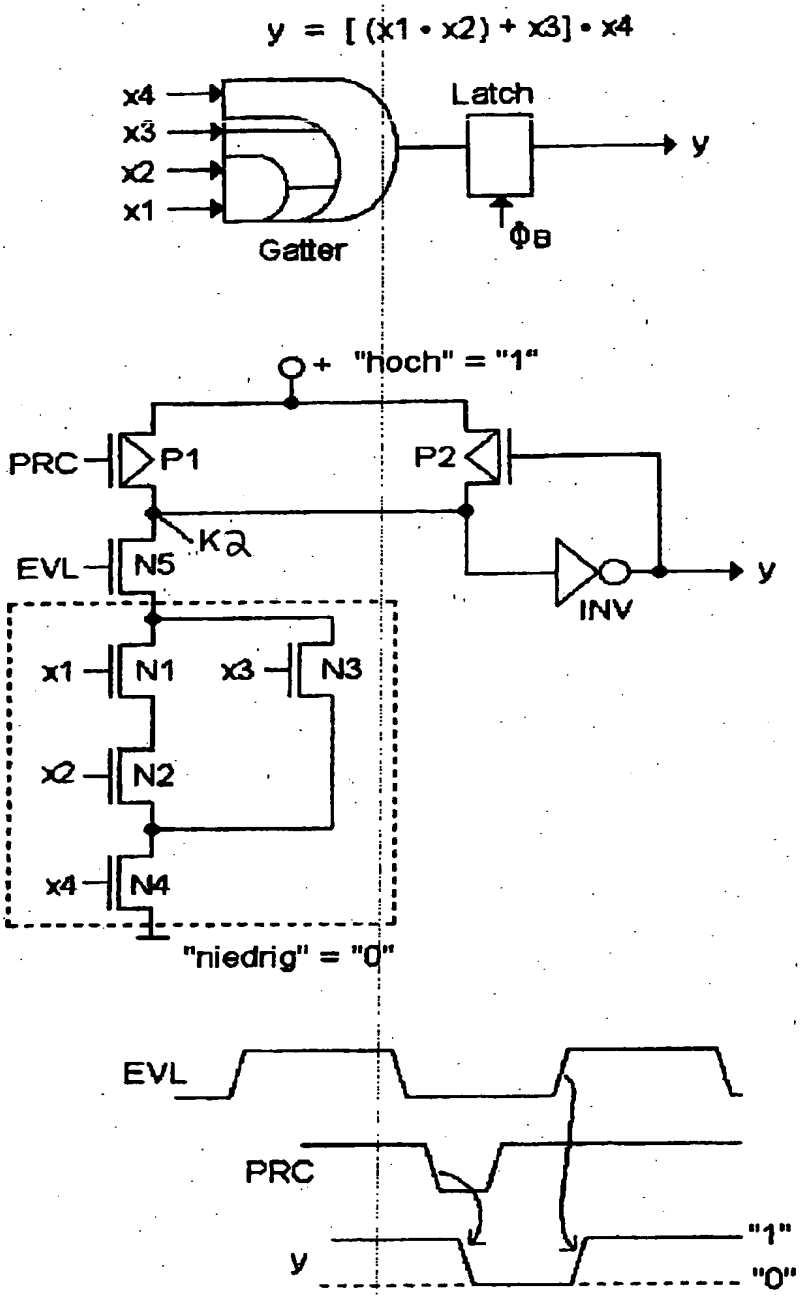
y = [(x1 • x2) + x3] • x4
x4
x3
x2
x1
Gatter
Latch
y
ΦB
+ "hoch" = "1"
PRC
P1
P2
K2
EVL
N5
INV
y
x1
N1
x3
N3
x2
N2
x4
N4
"niedrig" = "0"
EVL
PRC
y
"1"
"0"

Fig. 14